

IN THE CLAIMS

1       1. (original) A method for testing the design of an integrated circuit (system IC)  
2 comprising the steps of:

3             (a) designing the system IC to have a predetermined number and pattern for its  
4 chip I/O pads;  
5             (b) designing a packaging module to fan-out the I/O of the system IC to an  
6 expanded pitch of packaging I/O pads having a correspondence to said chip I/O pads;  
7             (c) partitioning circuitry of said system IC into a functional circuit;  
8             (d) designing said functional circuit as a corresponding test IC, wherein said test  
9 IC I/O pads conform to one of a sub-set of the number and pattern of said chip I/O pads;  
10            (e) attaching said test IC to said packaging module with conductive material;  
11            (f) exercising said test IC by applying signals and power to inputs of said  
12 packaging module at packaging I/O pads corresponding to said sub-set of chip I/O pads;  
13           and  
14             (g) collecting test data corresponding to said test IC.

15       2. (original) A method for testing the design of an integrated circuit (system IC)  
16 comprising the steps of:

17             (a) designing said system IC to have a predetermined number and pattern for its  
18 chip I/O pads;  
19             (b) designing a packaging module to fan-out the chip I/O to an expanded pitch of  
20 packaging I/O pads having a correspondence to said chip I/O pads;  
21             (c) partitioning functionality of said system IC into a plurality of individual  
22 functional circuits;  
23             (d) designing said plurality of individual functional circuits as a corresponding  
24 plurality of test ICs, wherein each of the test ICs conforms to one of a plurality of sub-  
25 sets of chip I/O pads making up said number and pattern of said chip I/O pads;

26                   (e) attaching said plurality of test ICs to said packaging module with conductive  
27 material;

28                   (f) interconnecting an I/O of a first test IC of said plurality of test ICs to an I/O of  
29 a second test IC of said plurality of test ICs external to said packaging module;

30                   (g) operating said plurality of test ICs by applying signals and power to selected  
31 ones of said packaging I/O pads corresponding to said plurality of sub-sets of said  
32 number and pattern of said chip I/O pads; and

33                   (h) collecting test data corresponding to operating said plurality of test ICs.

1       3. (original) The method of claim 2 further comprising the steps of:

2                   redesigning a first test IC of said plurality of test ICs generating a redesigned first  
3 test IC in response to said test data;

4                   replacing a corresponding one of said plurality of tests chips with said redesigned  
5 first test IC; and

6                   repeating steps (e)–(g).

1       4. (original) The method of claim 2 further comprising the step of:

2                   redesigning said functionality of said system IC in response to said test data.

1       5. (original) The method of claim 2 further comprising the steps of:

2                   coupling said system IC onto a PCB for a system designed to use said system IC;  
3 and

4                   operating said system IC to emulate at least one function of said system.

1       6. (original) The method of claim 2 further comprising the step of:

2                   testing said system IC in a test fixture designed for said system IC.

1        7. (original) A test module for a production system IC having a particular number and  
2        pattern of chip I/O pads, comprising:

3              a test IC corresponding to a sub-set of a total functionality of said system IC, said  
4        test IC having a test IC I/O configuration corresponding to a sub-set of said particular  
5        number and pattern of chip I/O pads;

6              a packaging module designed for said production system IC, having a packaging  
7        I/O number and pattern of packaging I/O pads for receiving said particular number and  
8        pattern of chip I/O pads;

9              couplings for electrically coupling said test IC I/O configuration to selected ones  
10       of said packaging I/O pads corresponding to said sub-set of said particular number and  
11       pattern of chip I/O pads; and

12        couplings for electrically coupling test signals to said selected ones of said  
13       packaging I/O pads corresponding to said sub-set of said particular number and pattern of  
14       chip I/O pads.

1        8. (original) A test module for a production system IC having a particular number and  
2        pattern of chip I/O pads, comprising:

3              a plurality of test ICs corresponding to a sub-set of a total functionality of said  
4        system IC, each of said plurality of test ICs having a test IC I/O configuration  
5        corresponding to an individual sub-set of said particular number and pattern of chip I/O  
6       pads;

7              a packaging module designed for said production system IC, having a number and  
8        pattern of packaging system IC pads for receiving said particular number and pattern of  
9       chip I/O pads, said packaging module having packaging I/O pads;

10        couplings for electrically coupling said test IC I/O configuration of each of said  
11       plurality of test ICs to selected ones of said packaging I/O pads corresponding to said  
12       sub-set of said particular number and pattern of chip I/O pads; and

13        couplings for electrically coupling test signals to said selected ones of said  
14       packaging I/O pads corresponding to said sub-set of said particular number and pattern of  
15       chip I/O pads.